FAIRCHILD SEMICONDUCTOR™

August 2001
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74VCX32245
Low Voltage 32-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs (Preliminary)

General Description

The VCX32245 contains thirty-two non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 32-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 74VCX32245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX32245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
  - 2.5 ns max for 3.0V to 3.6V V_{CC}
  - 3.0 ns max for 2.3V to 2.7V V_{CC}
  - 6.0 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  - ±24 mA @ 3.0V V_{CC}
  - ±18 mA @ 2.3V V_{CC}
  - ±6 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

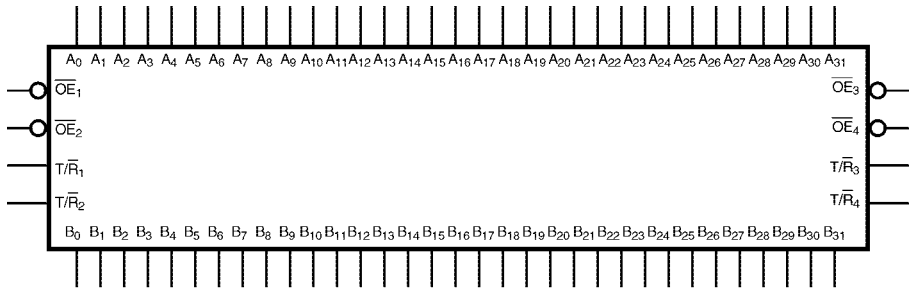
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

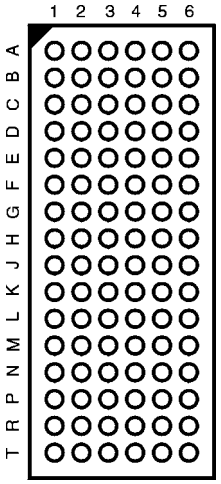
Order Number	Package Number	Package Description
74VCX32245GX (Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]

Note 2: BGA package available in Tape and Reel only.

Logic Symbol



Connection Diagram



(Top Thru View)

Truth Tables

Inputs $\overline{OE}_1$	Inputs $T/\overline{R}_1$	Outputs
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs $\overline{OE}_2$	Inputs $T/\overline{R}_2$	Outputs
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

Inputs $\overline{OE}_3$	Inputs $T/\overline{R}_3$	Outputs
L	L	Bus B_{16}–B_{23} Data to Bus A_{16}–A_{23}
L	H	Bus A_{16}–A_{23} Data to Bus B_{16}–B_{23}
H	X	HIGH Z State on A_{16}–A_{23}, B_{16}–B_{23}

Inputs $\overline{OE}_4$	Inputs $T/\overline{R}_4$	Outputs
L	L	Bus B_{24}–B_{31} Data to Bus A_{24}–A_{31}
L	H	Bus A_{24}–A_{31} Data to Bus B_{24}–B_{31}
H	X	HIGH Z State on A_{24}–A_{31}, B_{24}–B_{31}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
Z = High Impedance

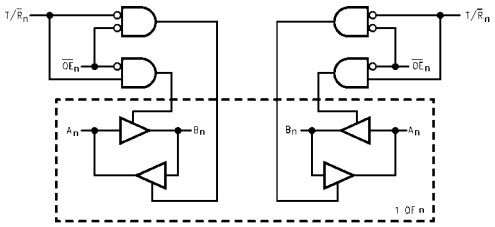
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{31}	Side A Inputs or 3-STATE Outputs
B_0–B_{31}	Side B Inputs or 3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_1	B_0	$T/\overline{R}_1$	$\overline{OE}_1$	A_0	A_1
B	B_3	B_2	GND	GND	A_2	A_3
C	B_5	B_4	V_{CC}	V_{CC}	A_4	A_5
D	B_7	B_6	GND	GND	A_6	A_7
E	B_9	B_8	GND	GND	A_8	A_9
F	B_{11}	B_{10}	V_{CC}	V_{CC}	A_{10}	A_{11}
G	B_{13}	B_{12}	GND	GND	A_{12}	A_{13}
H	B_{14}	B_{15}	$T/\overline{R}_2$	$\overline{OE}_2$	A_{15}	A_{14}
J	B_{17}	B_{16}	$T/\overline{R}_3$	$\overline{OE}_3$	A_{16}	A_{17}
K	B_{19}	B_{18}	GND	GND	A_{18}	A_{19}
L	B_{21}	B_{20}	V_{CC}	V_{CC}	A_{20}	A_{21}
M	B_{23}	B_{22}	GND	GND	A_{22}	A_{23}
N	B_{25}	B_{24}	GND	GND	A_{24}	A_{25}
P	B_{27}	B_{26}	V_{CC}	V_{CC}	A_{26}	A_{27}
R	B_{29}	B_{28}	GND	GND	A_{28}	A_{29}
T	B_{30}	B_{31}	$T/\overline{R}_4$	$\overline{OE}_4$	A_{31}	A_{30}

Logic Diagram



Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 4)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0V ≤ V_I ≤ 3.6V	2.7–3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0V ≤ V_O ≤ 3.6V; V_I = V_{IH} or V_{IL}	2.7–3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		40	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 6)	2.7–3.6		±40	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7–3.6		750	µA

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($2.3V \le V_{CC} \le 2.7V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3–2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\ \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3–2.7 2.3 2.3 2.3	$V_{CC} - 0.2$ 2.0 1.8 1.7		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu A$ $I_{OL} = 12$ mA $I_{OL} = 18$ mA	2.3–2.7 2.3 2.3		0.2 0.4 0.6	V
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	2.3–2.7		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.3–2.7		±10	µA
I_{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 7)	2.3–2.7 2.3–2.7		40 ±40	µA

Note 7: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($1.65V \le V_{CC} < 2.3V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65-2.3	$0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		1.65-2.3		$0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\ \mu A$ $I_{OH} = -6$ mA	1.65-2.3 1.65	$V_{CC} - 0.2$ 1.25		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu A$ $I_{OL} = 6$ mA	1.65-2.3 1.65		0.2 0.3	V
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65-2.3		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	1.65-2.3		±10	µA
I_{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 8)	1.65-2.3 1.65-2.3		40 ±40	µA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Prop Delay	0.8	2.5	1.0	3.0	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	0.8	3.8	1.0	4.9	1.5	9.3	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	0.8	3.7	1.0	4.2	1.5	7.6	ns

Note 9: For $C_L = 50$pF, add approximately 300ps to the AC maximum specification.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	–0.25	V
			2.5	–0.6	
			3.3	–0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8V$, 2.5V, or 3.3V, $V_I = 0V$ or V_{CC}	6	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$, or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, F = 10 MHz $V_{CC} = 1.8V$, 2.5V or 3.3V	20	pF

AC Loading and Waveforms

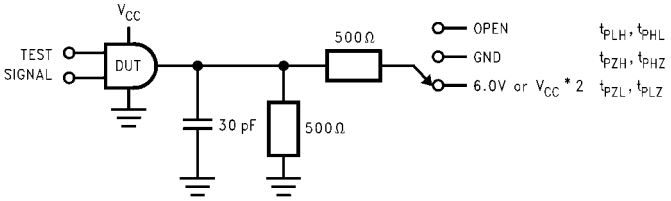


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

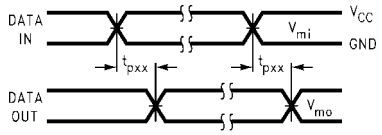


FIGURE 2. Waveform for Inverting and Non-inverting Functions

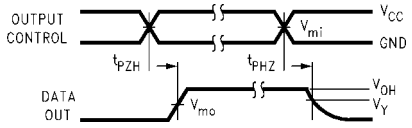


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

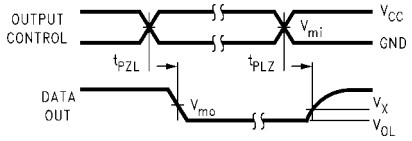
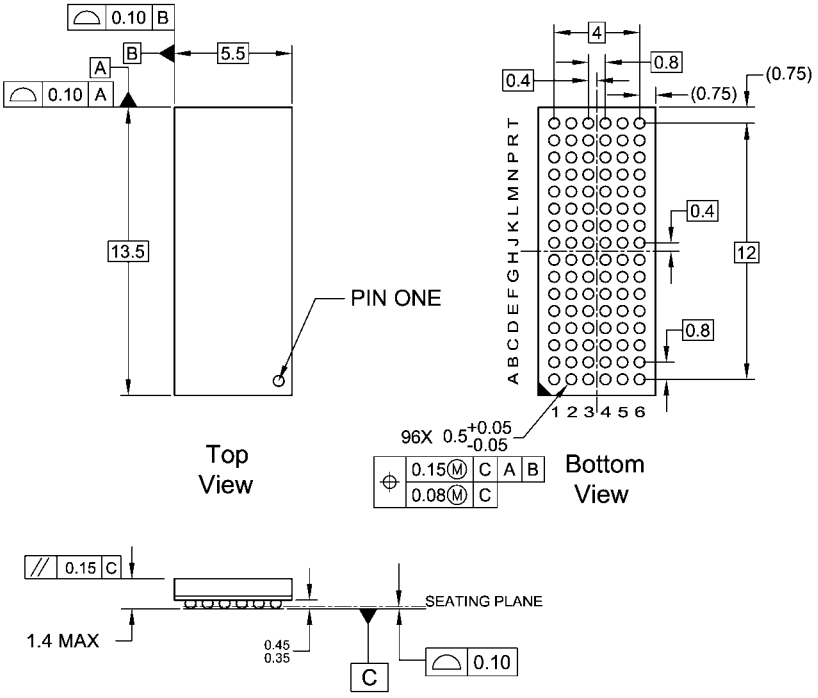


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A

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